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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/386,646	08/31/1999	PIERRE C. FAZAN	660073.488D1	1639

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/386,646	FAZAN ET AL.	
	Examiner	Art Unit	
	Hung K. Vu	2811	

-- Th MAILING DATE of this communication appears on th cover sh et with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22 and 24-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22 and 24-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the device further comprising a thin layer of oxide formed on the silicide layer, as recited in claims 25 and 41, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 22 and 24-43 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not disclose a field oxide layer extends above adjacent structures on the upper surface of the substrate, as recited in claim 22.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 26-34 and 39-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 26, 28, 30 and 34, the phrases "at least some of any adjacent structures" are unclear as to whether they are being referred to portions of adjacent structures or some of adjacent structures.

In claim 32, the phrase "at least some of gate structure" is unclear as to whether it is being referred to a portion of the gate structure or some of gate structures.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 28, 29, 32 and 33, insofar as incompliance with 35 USC 112, are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art Figure 1.

Applicant's Admitted Prior Art Figure 1 discloses a microelectronic device comprising:

a silicon substrate (20) having a trench formed in a surface thereof, the trench extending into the substrate substantially perpendicularly to the surface of the substrate;

a field oxide (60) in the trench, the field oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the

substantially straight sides extend from the trench beyond the surface of the substrate and above at least some adjacent structures or gate structure (gate oxide 30) on the upper surface of the substrate, the substantially straight sides extending substantially perpendicularly to the surface of the substrate and not extending laterally from the trench over the surface of the substrate;

a gate structure (100,300) formed on the substrate, the gate structure extending from the upper surface of the substrate by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the field oxide not contacting any portion of the gate structure.

With regard to claims 29 and 33, Applicant's Admitted Prior Art Figure 1 discloses the device further comprising an oxide spacer (91,93) adjacent the gate structure.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26-27, 30-31 and 39-43, insofar as incompliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art Figure 1 in view of Park et al. (PN 5,296,400, of record).

Applicant's Admitted Prior Art Figure 1 discloses a microelectronic device comprising:

a silicon substrate (20) having a trench formed in a surface thereof, the trench extending into the substrate substantially perpendicularly to the surface of the substrate and being bounded on all sides by the substrate;

a field oxide (60) in the trench, the field oxide having sides that are substantially straight and substantially parallel from a bottom of the trench to a top surface of the field oxide, the substantially straight sides projecting outwardly from the trench beyond the surface of the substrate and beyond at least some of any adjacent structures on the surface of the substrate, the substantially straight sides of the field oxide projecting substantially perpendicularly to the surface of the substrate and not extending laterally from the trench over the surface of the substrate;

a component (200) formed on the field oxide, the component comprising an adhesion layer (70) formed on the field oxide and a conductive silicide layer (80) formed on the adhesion layer.

Applicant's Admitted Prior Art Figure 1 does not disclose the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends beyond the surface of the substrate. However, Park et al. discloses a component (5) extending from the field oxide (3) by a height at least equal to approximately two times a height that the field oxide extends beyond the surface of the substrate. Note Figures 1F and 2H of Park et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the component of Applicant's Admitted Prior Art Figure 1 extending from the field oxide by a height at least equal to approximately two times a height that

the field oxide extends beyond the surface of the substrate, such as taught by Part et al. in order to increase the conductivity of the component.

With regard to claims 27 and 31, Applicant's Admitted Prior Art Figure 1 and Park et al. discloses the device further comprising an oxide spacer (7) adjacent the component.

With regard to claims 39 and 42, Applicant's Admitted Prior Art Figure 1 and Park et al. discloses the device further comprising a gate structure including a gate oxide layer formed on the upper surface of the substrate, the gate structure extending from the upper surface of the substrate to a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the filed oxide not contacting any portion of the gate structure.

With regard to claim 40, Applicant's Admitted Prior Art Figure 1 and Park et al. do not disclose the silicide layer comprising tungsten silicide.

With regard to claim 41, Applicant's Admitted Prior Art Figure 1 and Park et al. disclose the device further comprising a thin layer oxide (6) formed on the silicide layer.

6. Claims 26-34 and 39-43, insofar as incompliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (PN 5,296,400, of record) in view of Poppert et al. (PN 4,593,459, of record) and further in view of Lin et al. (PN 5,318,924).

Park et al. discloses, as shown in Figures 1F and 2H, a microelectronic device comprising,

a microelectronic substrate (1);

a gate structure formed on the substrate, the gate structure including a gate oxide layer (4) formed on the microelectronic substrate, a first gate layer (lower portion of 5) formed on the gate oxide layer, and an adhesion layer (upper portion of 5) formed on the first gate layer, the gate structure having a field oxide layer (3) at least partially disposed therein and extending into the substrate;

the field oxide layer not contact the gate oxide layer, the field oxide layer having a field oxide level between the level of the upper surface of the substrate and the level of an upper surface of the first gate layer.

a component formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the surface of the substrate;

Park et al. discloses the field oxide is a LOCOS. Park et al. does not disclose the field oxide is a trench isolation. However, Poppert et al. discloses a microelectronic device comprising a trench isolation (46,47). Note Figure 10 of Poppert et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the field oxide of Park et al. by trench isolation, such as taught by Poppert et al. in order to prevent the bird-beak effect and further isolate the devices from each others.

Park et al. and Poppert et al. do not disclose the structure further comprising a silicide layer formed on the adhesion layer. However, Lin et al. discloses a silicide layer (32) formed on the adhesion layer (26). Note Figure 6 of Lin et al.. Therefore, it would have been obvious to one of

ordinary skill in the art at the time the invention was made to form the device of Park et al. and Poppert et al. having a silicide layer on the adhesion layer, such as taught by Lin et al. in order to further reduce the contact resistance.

With regard to claims 27, 31 and 33, Park et al., Poppert et al. and Lin et al. disclose the device further comprising an oxide spacer (7) adjacent the component.

With regard to claims 28, 32 and 39, Park et al., Poppert et al. and Lin et al. disclose a gate structure formed on the substrate, the gate structure including a gate oxide layer formed on the microelectronic substrate, the gate structure extending from the upper surface of the substrate by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate, the filed oxide not contacting any portion of the gate structure.

With regard to claim 40, Park et al., Poppert et al. and Lin et al. discloses the silicide comprising titanium silicide. Park et al., Poppert et al. and Lin et al. do not disclose the silicide layer comprises tungsten silicide. However, at Col. 4, lines 44-49, other refractory metals can be used in place of titanium. It is well-known that other refractory metals include tungsten. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute titanium with tungsten, since titanium and tungsten are both considered to be an art recognized functional equivalent as the refractory metal silicide material for semiconductor device.

With regard to claim 41, Park et al., Poppert et al. and Lin et al. disclose the device further comprising a thin layer oxide (6) formed on the silicide layer.

7. Claim 28-29 and 32-34, insofar as incompliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi et al. (PN 4,935,802, of record) in view of Poppert et al. (PN 4,593,459, of record) and further in view of Lin et al. (PN 5,318,924). Noguchi et al. discloses, as shown in Figures 1 and 4, a microelectronic device comprising,

a microelectronic substrate (5);

a gate structure including a gate oxide layer (2) formed on the substrate, a first gate layer (3) formed on the gate oxide layer, and an adhesion layer (2) formed on the first gate layer, and a conductive layer (3) formed on the adhesion layer;

the field oxide layer (4) extending beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate, the field oxide layer not contact the gate oxide layer and not extending laterally over the surface of the substrate.

Noguchi discloses the field oxide is a LOCOS. Noguchi et al. does not disclose the field oxide is a trench isolation. However, Poppert et al. discloses a microelectronic device comprising a trench isolation (46,47). Note Figure 10 of Poppert et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the field oxide of Noguchi et al. by trench isolation, such as taught by Poppert et al. in order to prevent the bird-beak effect and further isolate the devices from each others.

Noguchi et al. and Poppert et al. do not disclose the conductive layer is a silicide layer. However, Lin et al. one may use a silicide layer (32) in place of conductive layer. Note Figure 6 of Lin et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the conductive layer of Noguchi et al. and Poppert et al. with a silicide layer, such as taught by Lin et al. in order to further reduce the contact resistance.

With regard to claims 29, 31, and 33, Noguchi et al. does not disclose an oxide spacer adjacent the gate structure. However, Poppert et al. or Lin et al. discloses an oxide spacer (62) adjacent the gate structure. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate structure of Noguchi et al. having an oxide spacer, such as taught by Poppert et al. or Lin et al. in order to protect the gate and the source/drain region from short-circuit.

Response to Arguments

8. Applicant's arguments filed 04/14/02 have been fully considered but they are not persuasive.

Applicant's amendment to claims 26, 28, 30, 32 and 34 by incorporating the phrase "at least some of", "at least some of any", or "at least some of the gate", necessitated the new ground(s) of rejection presented in this Office action. Accordingly, this action is made final.

It is argued, at pages 7-9 of the Remarks, that the subject matter of claims 22, 26, 28, 30, 32 and 34 are most clearly shown in Figure 2G which discloses the "adjacent structures" as being the

gate oxide layer 30 and a portion of the first gate layer 40. This argument is not convincing because the specification does not mention that both the gate oxide layer 30 and the portion of the first gate layer 40 are the adjacent structures. The claimed language only mentions about the gate structure and specifically states that the gate structure includes a gate oxide layer and/or a first gate layer, etc., therefore, the gate oxide layer 30 and the first gate layer 40 are portions of the gate structure, and the field oxide layer does not extend above gate structures. Therefore, adjacent to the isolation structure is the gate structure. Further, the ordinary meaning of the word "adjacent" is normally implied that there is nothing in between. As applied to this case, the gate oxide layer 30 and the first gate layer are not adjacent to the field oxide layer because there are the spacers 91 and 93 in between.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 7:00-4:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

July 6, 2003

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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